Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor integrated circuit device comprising:

register circuits which receive data signals, an output timing of each of the register circuits being controlled by a clock signal;

a delay adjustment signal output circuit which receives the data signals and outputs delay adjustment signals based on the data signals;

delay adjustment circuits which receive outputs of the register circuits and output delay adjusted data signals, a delay time of each of the delay adjustment circuits being adjusted based on the delay adjustment signals; and

~~the~~ driver circuits which receive the delay adjusted data signals,

wherein values of the delay adjustment signals change in accordance with ~~data pattern~~ logical combinations of the data signals.

2. (Previously presented) The device according to claim 1, wherein the data signals are read data signals, and the driver circuits are off-chip driver circuits.

3. (Previously presented) The device according to claim 1, wherein the data signals are write data signals, and the driver circuits are write data buffer circuits.

4. (Previously presented) The device according to claim 1, wherein the data signals are address signals, and the driver circuits are address buffer circuits.

5. (Currently amended) A semiconductor integrated circuit device comprising:

a delay adjustment signal output circuit which receives the data signals and outputs delay adjustment signals based on the data signals;

delay adjustment circuits which receive a clock signal and output delay adjusted clock signals, delay times of the delay adjustment circuits being adjusted based on the delay adjustment signals;

register circuits which receive the data signals, an output timing of each of the register circuits being controlled by the delay adjusted clock signals; and

driver circuits which receive outputs of the register circuits,

wherein values of the delay adjustment signals change in accordance with ~~data pattern~~ logical combinations of the data signals.

6. (Previously presented) The device according to claim 5, wherein the data signals are read data signals, and the driver circuits are off-chip driver circuits.

7. (Currently amended) A semiconductor integrated circuit device comprising:

a first register circuit which receives a first data signal;

a second register circuit which receives a second data signal;

a delay adjustment signal output circuit which receives the first and second data signals and outputs a delay adjustment signal based on the first and second data signals;

a first delay adjustment circuit which receives an output of the first register circuit and outputs a first delay adjusted data signal, a delay time of the first delay adjustment circuit being adjusted based on the delay adjustment signal;

a second delay adjustment circuit which receives an output of the second register circuit and outputs a second delay adjusted data signal, a delay time of the second delay adjustment circuit being adjusted based on the delay adjustment signal;

a first driver circuit which receives the first delay adjusted data signal; and

a second driver circuit which receives the second delay adjusted data signal,

wherein a value of the delay adjustment signal changes in accordance with ~~data pattern~~ logical combinations of the first and second data signals.

8. (Previously presented) The device according to claim 7, wherein the first and second data signals are read data signals, and the first and second driver circuits are off-chip driver circuits.

9. (Previously presented) The device according to claim 7, wherein the first and second data signals are write data signals, and the first and second driver circuits are write data buffer circuits.

10. (Previously presented) The device according to claim 7, wherein the first and second data signals are address signals, and the first and second driver circuits are address buffer circuits.

11-13. (Canceled)